ESP8684 Series

Datasheet Version 2.3

RISC-V Single-Core CPU
2.4 GHz Wi-Fi (IEEE 802.11b/g/n) and Bluetooth® 5 (LE)
Optional 2 MB or 4 MB flash in the chip's package
14 GPIOs
QFN24 (4×4 mm) Package

Including:

ESP8684H2X (The upgraded version of ESP8684H2)

ESP8684H4X (The upgraded version of ESP8684H4)

NOTE:

The ESP8684 chip series belongs to the ESP32-C2 group. Currently, the ESP32-C2 group consists of only one series, the ESP8684.

ESPRESSIF

Product Overview

ESP8684 series of SoCs is an ultra-low-power and highly-integrated MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE).

The functional block diagram of the SoC is shown below.

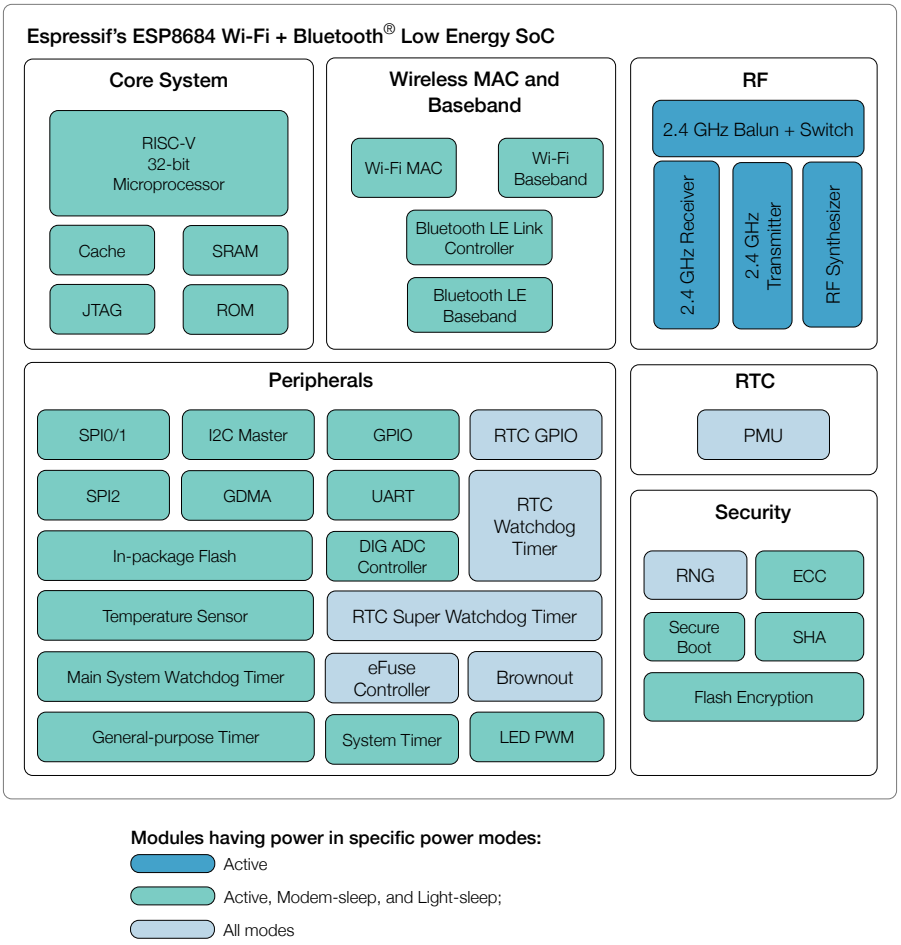


Figure 1: ESP8684 Functional Block Diagram

For more information on power consumption, see Section 4.1.3.6 *Power Management Unit*.

Features

Wi-Fi

- Complies with IEEE 802.11b/g/n
- Supports 20 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 72.2 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- Three virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
  Note that when ESP8684 series scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity

Bluetooth

- Bluetooth LE: Bluetooth 5.3 certified
- High power mode (20 dBm)
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

CPU and Memory

- 32-bit RISC-V single-core processor, up to 120 MHz
- CoreMark® score:
  - One core at 120 MHz: 369.58 CoreMark; 3.08 CoreMark/MHz
- 576 KB ROM
- 272 KB SRAM (16 KB for cache)
- In-package flash (see details in Chapter 1 *ESP8684 Series Comparison*)

- Access to flash accelerated by cache
- Supports flash in-Circuit Programming (ICP)

Advanced Peripheral Interfaces

- 14 programmable GPIOs
  - 2 strapping GPIOs
- Digital interfaces:
  - Three SPI
  - Two UART
  - I2C Master
  - LED PWM controller, with up to 6 channels
  - General DMA controller (GDMA), with 1 transmit channel and 1 receive channel
- Analog interfaces:
  - 12-bit SAR ADC, up to 5 channels
  - Temperature sensor
- Timers:
  - 54-bit general-purpose timer
  - Two watchdog timers
  - 52-bit system timer

Low Power Management

- Fine-resolution power control through a selection of clock frequency, duty cycle, Wi-Fi operating modes, and individual power control of internal components
- Four power modes designed for typical scenarios: Active, Modem-sleep, Light-sleep, Deep-sleep
- Power consumption in Deep-sleep mode is 5 μA
- RTC memory remains powered on in Deep-sleep mode

Security

- Secure boot - permission control on accessing internal and external memory
- Flash encryption - memory encryption and decryption
- 1024-bit OTP, up to 256 bits for users
- Cryptographic hardware acceleration:
  - ECC
  - SHA Accelerator (FIPS PUB 180-4)
- Random Number Generator (RNG)

- Clock glitch filter

RF Module

- Antenna switches, RF balun, power amplifier, low-noise receive amplifier
- Up to +22 dBm of power for an 802.11b transmission
- Up to +20 dBm of power for an 802.11n transmission
- Up to -106 dBm of sensitivity for Bluetooth LE receiver (125 Kbps)

Applications

With ultra-low power consumption, ESP8684 is an ideal choice for IoT devices in the following areas:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://www.espressif.com/documentation/esp8684_datasheet_en.pdf

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1 ESP8684 Series Comparison

1.1 Nomenclature

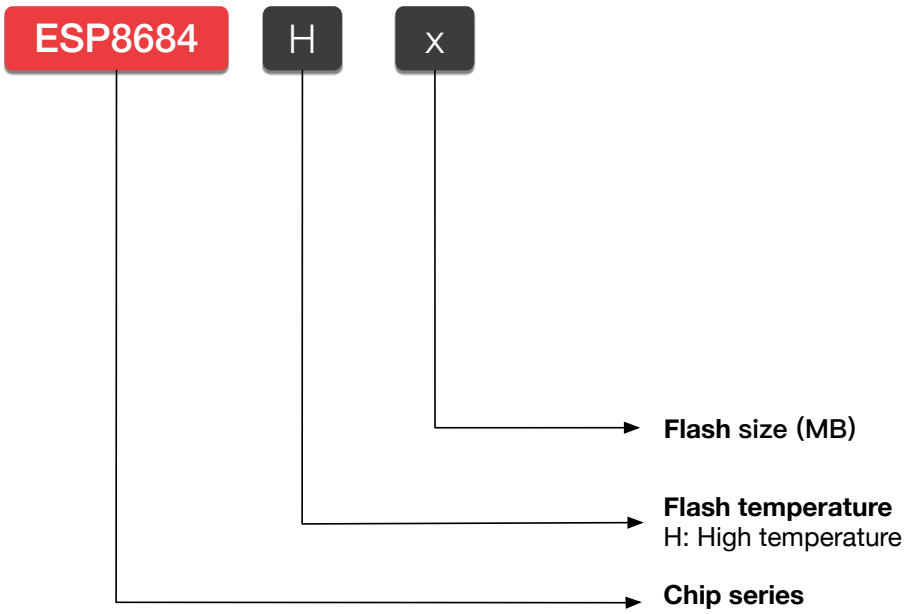


Figure 2: ESP8684 Series Nomenclature

1.2 Comparison

Table 1: ESP8684 Series Member Comparison

Part Number[1]	In-Package flash [2, 3]	Ambient Temperature[4] (°C)	Chip Revision [5]
ESP8684H2X [6]	2 MB	−40 ~ 105	v2.0
ESP8684H4X [6]	4 MB	−40 ~ 105	v2.0

[1] For details on chip marking and packing, see Section 7 *Packaging*.

[2] By default, the SPI flash on the chip operates at a maximum clock frequency of 60 MHz and does not support the auto suspend feature. If you need the flash auto suspend feature, please contact us.

[3] The in-package flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

[4] Ambient temperature specifies the recommended temperature range of the environment immediately outside an Espressif chip.

[5] Compared to previous chip versions, chip version v2.0 provides an additional 20 KB of SRAM and approximately 100 KB of flash memory (subject to actual application).

[6] ESP8684H2X and ESP8684H4X are upgraded versions of ESP8684H2 and ESP8684H4, respectively. The corresponding chip versions for ESP8684H2 and ESP8684H4 are v1.2 and earlier.

1.3 Chip Revision

As shown in Table 1 *Comparison*, ESP8684 now has multiple chip revisions available on the market using the same part number.

For chip revision identification, ESP-IDF release that supports a specific chip revision, and errors fixed in each chip revision, please refer to *ESP8684 Series SoC Errata*.

2 Pins

2.1 Pin Layout

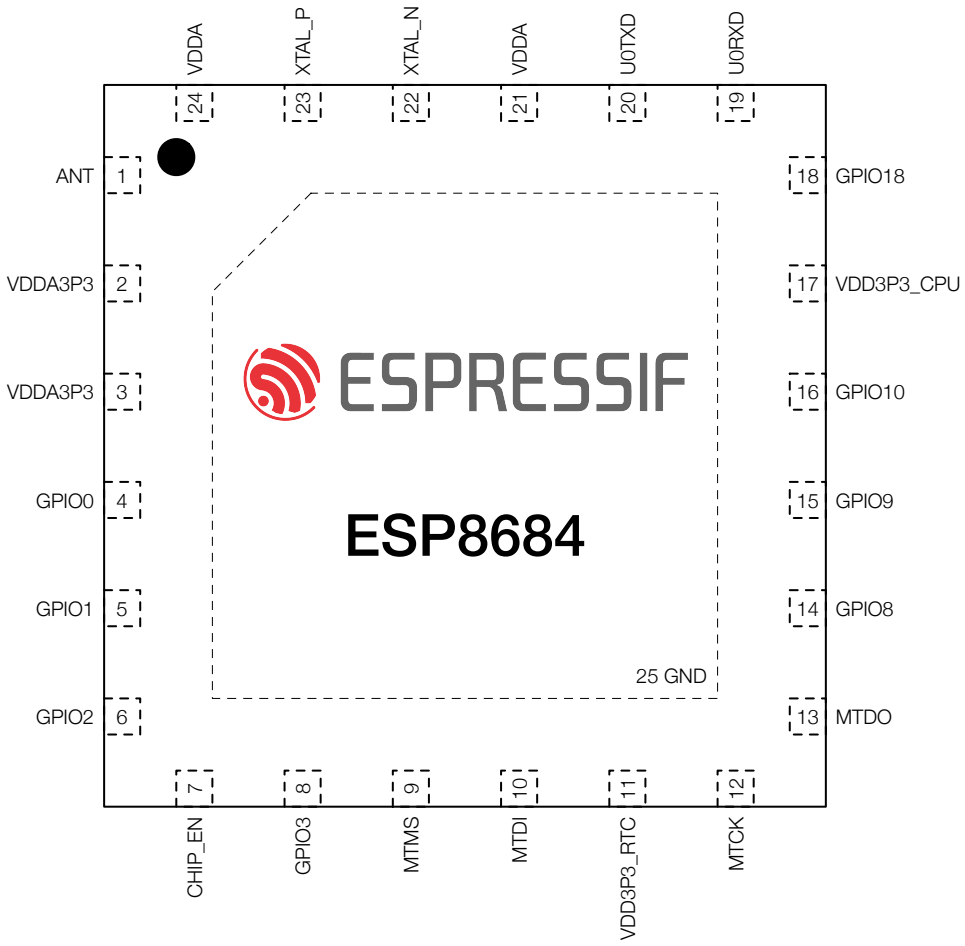


Figure 3: ESP8684 Pin Layout (Top View)

2.2 Pin Overview

The ESP8684 chip integrates multiple peripherals that require communication with the outside world. To keep the chip package size reasonably small, the number of available pins has to be limited. So the only way to route all the incoming and outgoing signals is through pin multiplexing. Pin muxing is controlled via software programmable registers (see *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*).

All in all, the ESP8684 chip has the following types of pins:

- **IO pins** with the following predefined sets of functions to choose from:
  - **Each** IO pin has predefined **IO MUX functions** – see Table 4 *IO MUX Functions*
  - **Some** IO pins have predefined **analog functions** – see Table 6 *Analog Functions*

  Predefined functions means that each IO pin has a set of direct connections to certain signals from on-chip peripherals. During run-time, the user can configure which peripheral signal from a predefined set to connect to a certain pin at a certain time via memory mapped registers.
- **Analog pins** that have exclusively-dedicated **analog functions** – see Table 7 *Analog Pins*
- **Power pins** that supply power to the chip components and non-power pins – see Table 8 *Power Pins*

Table 2 *Pin Overview* gives an overview of all the pins. For more information, see the respective sections for each pin type below, or Appendix A – ESP8684 Consolidated Pin Overview.

Table 2: Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power [2-3]	Pin Settings [4]		Pin Function Sets [1]	
				At Reset	After Reset	IO MUX	Analog
1	ANT	Analog	-				
2	VDDA3P3	Power	-				
3	VDDA3P3	Power	-				
4	GPIO0	IO	VDD3P3_RTC			**IO MUX**	Analog
5	GPIO1	IO	VDD3P3_RTC			**IO MUX**	Analog
6	GPIO2	IO	VDD3P3_RTC	IE	IE	**IO MUX**	Analog
7	CHIP_EN	IO	VDD3P3_RTC				
8	GPIO3	IO	VDD3P3_RTC	IE	IE	**IO MUX**	Analog
9	MTMS	IO	VDD3P3_RTC		IE	**IO MUX**	Analog
10	MTDI	IO	VDD3P3_RTC		IE	**IO MUX**	
11	VDD3P3_RTC	Power	-				
12	MTCK	IO	VDD3P3_CPU		IE	**IO MUX**	
13	MTDO	IO	VDD3P3_CPU		IE	**IO MUX**	
14	GPIO8	IO	VDD3P3_CPU	IE	IE	**IO MUX**	
15	GPIO9	IO	VDD3P3_CPU	IE	IE, WPU	**IO MUX**	
16	GPIO10	IO	VDD3P3_CPU			**IO MUX**	
17	VDD3P3_CPU	Power	-				
18	GPIO18	IO	VDD3P3_CPU			**IO MUX**	
19	U0RXD	IO	VDD3P3_CPU		IE, WPU	**IO MUX**	
20	U0TXD	IO	VDD3P3_CPU		OE, WPU	**IO MUX**	

Cont'd on next page

Table 2 – cont'd from previous page

Pin No.	Pin Name	Pin Type	Pin Providing Power [2-3]	Pin Settings [4]		Pin Function Sets [1]	
				At Reset	After Reset	IO MUX	Analog
21	VDDA	Power	-				
22	XTAL_N	Analog	-				
23	XTAL_P	Analog	-				
24	VDDA	Power	-				
25	GND	Power	-				

1. **Bold** marks the pin function set in which a pin has its default function in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.
2. In column **Pin Providing Power**, regarding pins powered by VDD3P3_CPU:
   - Pin Providing Power (either VDD3P3_CPU) can be configured via a register, see *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.
3. Default drive strength for all IO pins is 20 mA.
4. Column **Pin Settings** shows predefined settings at reset and after reset with the following abbreviations:
   - IE – input enabled
   - OE – output enabled
   - WPU – internal weak pull-up resistor enabled

2.3 IO Pins

2.3.1 IO MUX Functions

The IO MUX allows multiple input/output signals to be connected to a single input/output pin. Each IO pin of ESP8684 can be connected to one of the three signals (IO MUX functions, i.e., F0-F2), as listed in Table 4 *IO MUX Functions*.

Among the three sets of signals:

- Some are routed via the GPIO Matrix (**GPIO2, GPIO3, etc.**), which incorporates internal signal routing circuitry for mapping signals programmatically. It gives the pin access to almost any peripheral signals. However, the flexibility of programmatic mapping comes at a cost as it might affect the latency of routed signals. For details about connecting to peripheral signals via GPIO Matrix, see *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.
- Some are directly routed from certain peripherals (**U0TXD, MTCK, etc.**), see Table 3 *IO MUX Functions*.

Table 3: Peripheral Signals Routed via IO MUX

Pin Function	Signal	Description
U0TXD U0RXD	Transmit data Receive data	UART0 interface
MTCK MTDO MTDI MTMS	Test clock Test Data Out Test Data In Test Mode Select	JTAG interface for debugging
FSPIQ FSPID FSPIHD FSPIWP FSPICLK FSPICS0	Data out Data in Hold Write protect Clock Chip select	SPI2 interface for fast SPI connection. It supports 1-, 2-, 4-line SPI modes

Table 4 *IO MUX Functions* shows the IO MUX functions of IO pins.

Table 4: IO MUX Pin Functions

Pin No.	IO MUX / GPIO Name [2]	IO MUX Function [1]					
		F0	Type [3]	F1	Type	F2	Type
4	GPIO0	GPIO0	I/O/T	**GPIO0**	I/O/T		
5	GPIO1	GPIO1	I/O/T	**GPIO1**	I/O/T		
6	GPIO2	GPIO2	I/O/T	**GPIO2**	I/O/T	FSPIQ	I1/O/T
8	GPIO3	GPIO3	I/O/T	**GPIO3**	I/O/T		
9	GPIO4	**MTMS**	I1	GPIO4	I/O/T	FSPIHD	I1/O/T
10	GPIO5	**MTDI**	I1	GPIO5	I/O/T	FSPIWP	I1/O/T
12	GPIO6	**MTCK**	I1	GPIO6	I/O/T	FSPICLK	I1/O/T
13	GPIO7	**MTDO**	O/T	GPIO7	I/O/T	FSPID	I1/O/T

Cont'd on next page

Table 4 – cont'd from previous page

Pin No.	IO MUX / GPIO Name [2]	IO MUX Function [1]					
		F0	Type [3]	F1	Type	F2	Type
14	GPIO8	GPIO8	I/O/T	**GPIO8**	I/O/T		
15	GPIO9	GPIO9	I/O/T	**GPIO9**	I/O/T		
16	GPIO10	GPIO10	I/O/T	**GPIO10**	I/O/T	FSPICS0	I1/O/T
18	GPIO18	GPIO18	I/O/T	**GPIO18**	I/O/T		
19	GPIO19	**U0RXD**	I1	GPIO19	I/O/T		
20	GPIO20	**U0TXD**	O	GPIO20	I/O/T		

[1] **Bold** marks the default pin functions in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.

[2] Regarding highlighted cells, see Section 2.3.3 *Restrictions for GPIOs and RTC_GPIOs*.

[3] Each IO MUX function (F*n*, *n* = 0 ~ 2) is associated with a *type*. The description of *type* is as follows:

- I – input. O – output. T – high impedance.
- I1 – input; if the pin is assigned a function other than F*n*, the input signal of F*n* is always `1`.
- I0 – input; if the pin is assigned a function other than F*n*, the input signal of F*n* is always `0`.

2.3.2 Analog Functions

Some IO pins also have **analog functions**, for analog peripherals (such as ADC) in any power mode. Internal analog signals are routed to these analog functions, see Table 5 *Analog Functions*.

Table 5: Analog Signals Routed to Analog Functions

Pin Function	Signal	Description
ADC1_CH...	ADC1 channel ... signal	ADC1 interface

Table 6 *Analog Functions* shows the analog functions of IO pins.

Table 6: Analog Functions

Pin No.	Analog IO Name [1]	Analog Function [2]	
		F0	F1
4	GPIO0		ADC1_CH0
5	GPIO1		ADC1_CH1
6	GPIO2		ADC1_CH2
8	GPIO3		ADC1_CH3
9	GPIO4		ADC1_CH4

[1] **Bold** marks the default pin functions in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.

[2] This column lists the GPIO names, since analog functions are configured with GPIO registers that use GPIO numbering.

2.3.3 Restrictions for GPIOs and RTC_GPIOs

All IO pins of ESP8684 have GPIO. However, the IO pins are multiplexed and can be configured for different purposes based on the requirements. Some IOs have restrictions for usage. It is essential to consider the multiplexed nature and the limitations when using these IO pins.

In tables of this chapter, some pin functions are highlighted. The non-highlighted GPIO or RTC_GPIO pins are recommended for use first. If more pins are needed, the highlighted GPIOs or RTC_GPIOs should be chosen carefully to avoid conflicts with important pin functions.

The highlighted IO pins have the following important pin functions:

- GPIO – have one of the following important functions:
  - **Strapping pins** – need to be at certain logic levels at startup. See Section 3 *Boot Configurations*.
  - **JTAG interface** – often used for debugging. See Table 3 *IO MUX Functions*.
  - **UART interface** – often used for debugging. See Table 3 *IO MUX Functions*.

See also Appendix A – ESP8684 Consolidated Pin Overview.

2.4 Analog Pins

Table 7: Analog Pins

Pin No.	Pin Name	Pin Type	Pin Function
1	ANT	I/O	RF input and output
7	CHIP_EN	I	High: on, enables the chip (powered up). Low: off, disables the chip (powered down). Note: Do not leave the CHIP_EN pin floating.
22	XTAL_N	—	External clock input/output connected to ESP8684's crystal or oscillator. P/N means differential clock positive/negative.
23	XTAL_P	—	

2.5 Power Supply

2.5.1 Power Pins

The chip is powered via the power pins described in Table 8 *Power Pins*.

Table 8: Power Pins

Pin No.	Pin Name	Direction	Power Supply [1,2] Power Domain/Other	Power Supply [1,2] IO Pins [3]
2	VDDA3P3	Input	Analog power domain	
3	VDDA3P3	Input	Analog power domain	
11	VDD3P3_RTC	Input	RTC and part of Digital power domains	RTC IO
17	VDD3P3_CPU	Input	Digital power domain	Digital IO
21	VDDA	Input	Analog power domain	
24	VDDA	Input	Analog power domain	
25	GND	—	External ground connection	

[1] See in conjunction with Section 2.5.2 *Power Scheme*.

[2] For recommended and maximum voltage and current, see Section 5.1 *Absolute Maximum Ratings* and Section 5.2 *Recommended Operating Conditions*.

[3] RTC IO pins are those powered by VDD3P3_RTC and so on, as shown in Figure 4 *ESP8684 Power Scheme*. See also Table 2 *Pin Overview* > Column *Pin Providing Power*.

2.5.2 Power Scheme

The power scheme is shown in Figure 4 *ESP8684 Power Scheme*.

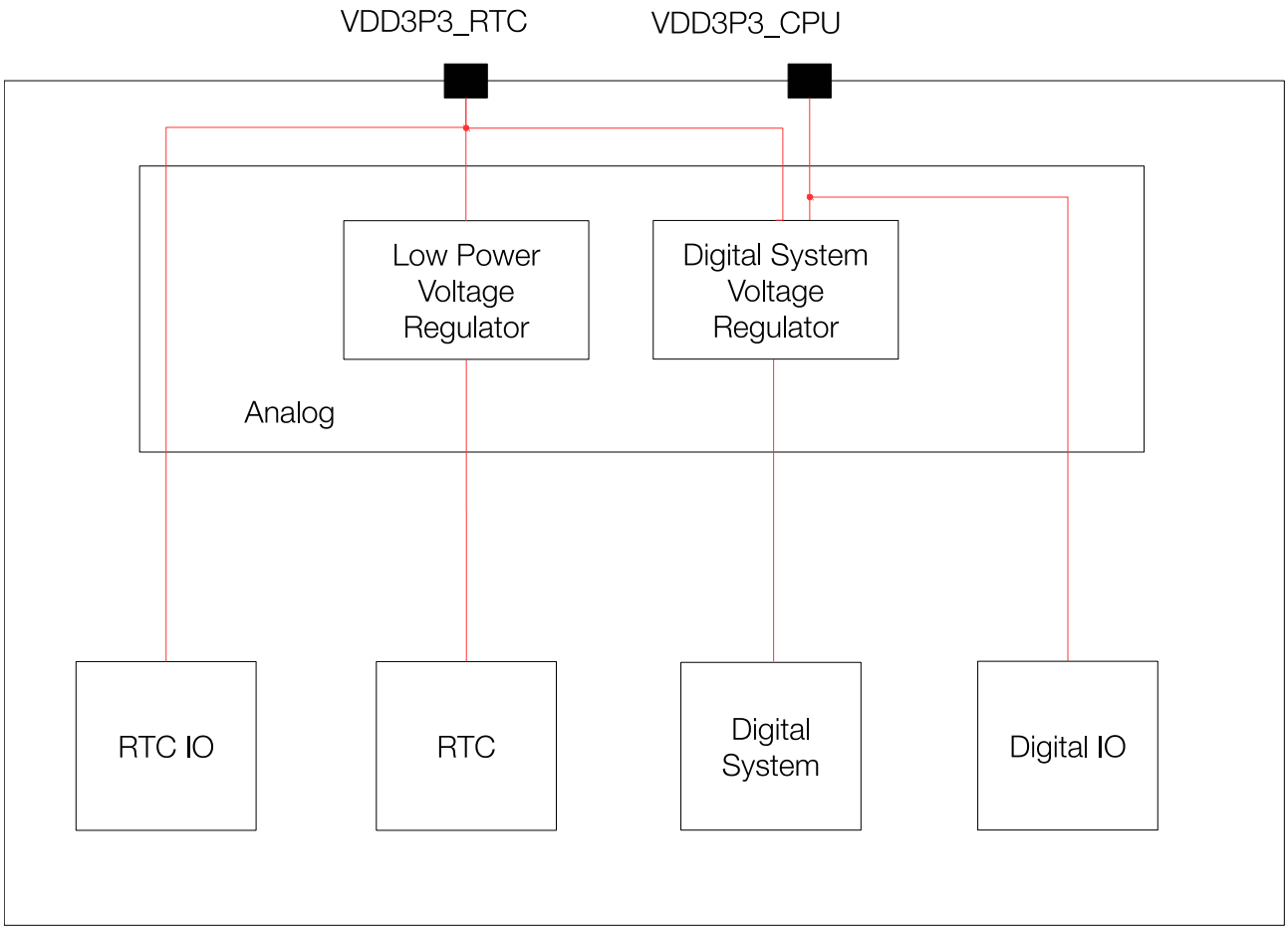


Figure 4: ESP8684 Power Scheme

2.5.3 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails need a short time to stabilize. After that, CHIP_EN – the pin used for power-up and reset – is pulled high to activate the chip. For information on CHIP_EN as well as power-up and reset timing, see Figure 5 and Table 9.

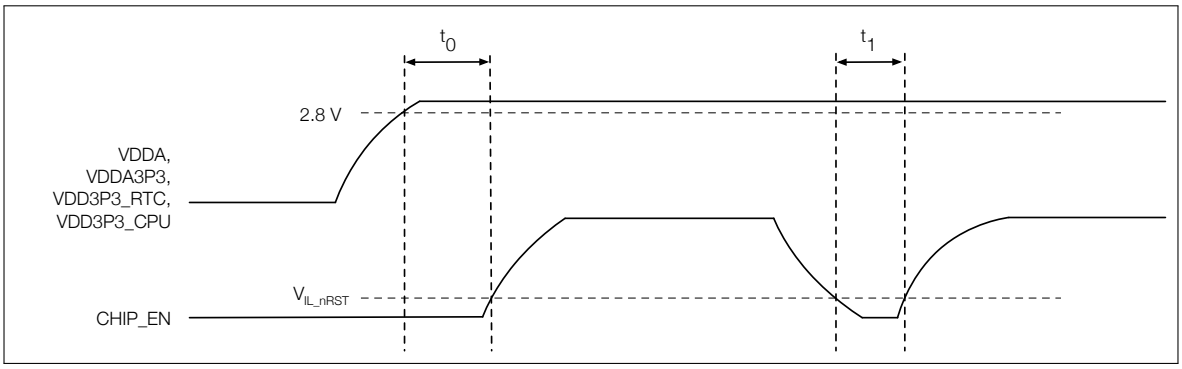


Figure 5: Visualization of Timing Parameters for Power-up and Reset

Table 9: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDDA3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} (refer to its value in Table 17) to reset the chip	50

3 Boot Configurations

The chip allows for configuring the following boot parameters through strapping pins and eFuse parameters at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO8 and GPIO9
- **ROM message printing**
  - Strapping pin: GPIO8
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP8684 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 10: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO8	N/A	-
GPIO9	Internal weak pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP8684 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 11 and Figure 6.

Table 11: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

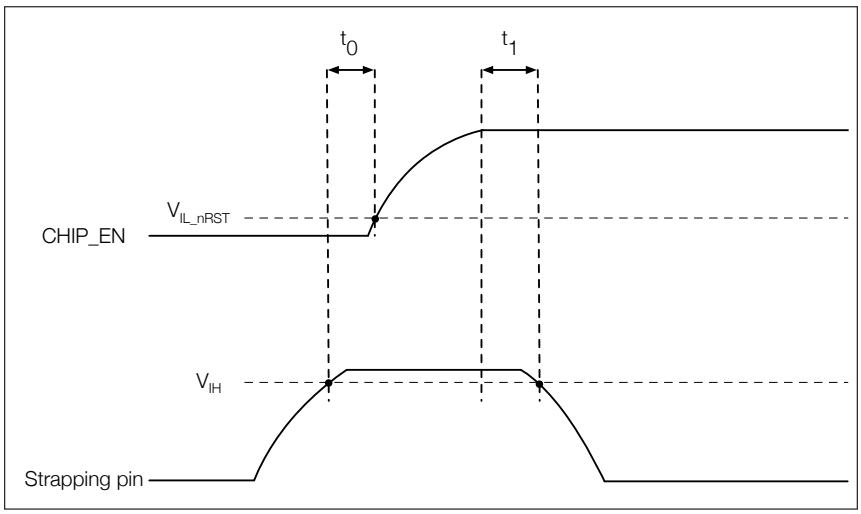


Figure 6: Visualization of Timing Parameters for the Strapping Pins

3.1 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 12 *Chip Boot Mode Control*.

Table 12: Chip Boot Mode Control

Boot Mode	GPIO9	GPIO8
SPI boot mode	1	x[2]
Joint download boot mode [3]	0	1

[1] **Bold** marks the default value and configuration.

[2] Values that have no effect on the result and can therefore be ignored.

[3] Joint Download Boot mode supports UART Download Boot. In addition to SPI Boot and Joint Download Boot modes, ESP8684 also supports SPI Download Boot mode. For details, please see *ESP8684 Technical Reference Manual* > Chapter *Chip Boot Control*.

3.2 ROM Messages Printing Control

EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table 13 *UART0 ROM Message Printing Control*.

Table 13: UART0 ROM Message Printing Control

UART0 ROM Code Printing	eFuse[1]	GPIO8
Enabled	**0**	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

[1] EFUSE_UART_PRINT_CONTROL

3.3 Crystal Frequency Selection

ESP8684 supports crystal frequencies of 26 MHz and 40 MHz.

The chip does not support automatic detection of the crystal frequency, nor is this information stored in EFUSE. Therefore, the correct frequency must be explicitly configured in software during development to ensure proper operation.

Upon power-on reset, the ROM bootloader assumes a default crystal frequency of 40 MHz and sets the UART baud rate to 115200 bps accordingly.

If a 26 MHz crystal is connected instead, the actual UART baud rate will be approximately 74880 bps. In this case, the external device must identify the correct crystal frequency by analyzing the UART waveform and adjust its baud rate accordingly for proper communication.

After the bootloader stage, the system must configure the main clock and initialize the required subsystem clocks based on the crystal frequency specified in software.

Note:
It is recommended to use the official software framework (e.g., ESP-IDF) to initialize clocks based on the crystal frequency. This ensures consistent and stable clock configuration across all subsystems.

4 Functional Description

4.1 System

This section describes the core of the chip's operation, covering its microprocessor, memory organization, system components, and security features.

4.1.1 Microprocessor and Master

This subsection describes the core processing units within the chip and their capabilities.

4.1.1.1 High-Performance CPU

The ESP-RISC-V CPU (HP CPU) is a high-performance 32-bit core based on the RISC-V instruction set architecture (ISA) comprising base integer (I), multiplication/division (M), atomic (A) and compressed (C) standard extensions.

Feature List

- Four-stage pipeline that supports an operating clock frequency up to 120 MHz
- RV32IMAC ISA (instruction set architecture)
- 32-bit multiplier and 32-bit divider
- Up to 32 vectored interrupts at seven priority levels
- Up to 2 hardware breakpoints/watchpoints
- JTAG for debugging

For details, see *ESP8684 Technical Reference Manual* > Chapter *High-Performance CPU*.

4.1.1.2 GDMA Controller

The GDMA Controller is a General Direct Memory Access (GDMA) controller that allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory data transfer with the CPU's intervention. The GDMA has two independent channels, one transmits and one receives. These channels are shared by peripherals with the GDMA feature, such as SPI2 and SHA.

Feature List

- Programmable length of data to be transferred in bytes
- Linked list of descriptors
- INCR burst transfer when accessing internal RAM for improved performance
- Access to an address space of up to 256 KB in internal RAM
- Onetransmit channel and one receive channel
- Software-configurable selection of peripheral requesting its service
- Fixed channel priority and round-robin channel arbitration

- AHB bus architecture

For details, see *ESP8684 Technical Reference Manual* > Chapter *GDMA Controller (DMA)*.

4.1.2 Memory Organization

This subsection describes the memory arrangement to explain how data is stored, accessed, and managed for efficient operation.

Figure 7 illustrates the address mapping structure of ESP8684.

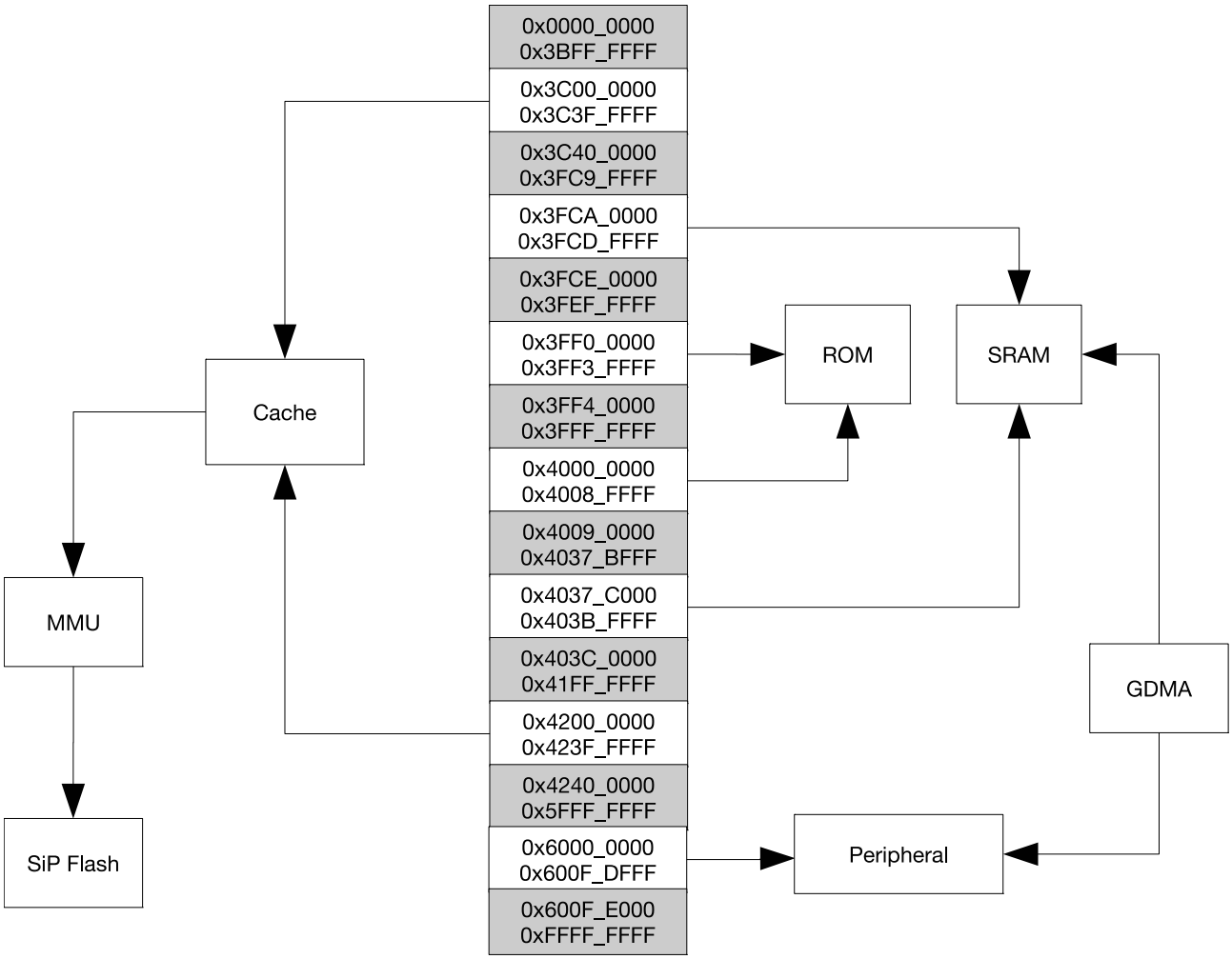


Figure 7: Address Mapping Structure

Note:
The memory space with gray background is not available for use.

4.1.2.1 Internal Memory

The internal memory of ESP8684 refers to the memory integrated on the chip die or in the chip package, including ROM, SRAM, eFuse, and flash.

Feature List

- 576 KB of ROM for booting and core functions
- 272 KB of on-chip SRAM for data and instructions, running at a configurable frequency of up to 120 MHz. Of the 272 KB SRAM, 16 KB is configured for cache.
- 1 Kbit eFuse memory, with 256 bits available for users. See also Section 4.1.2.3 *eFuse Controller*
- In-package flash
  - See flash size in Chapter 1 *ESP8684 Series Comparison*
  - More than 100,000 program/erase cycles
  - More than 20 years of data retention time
  - Clock frequency up to 60 MHz by default

For details, see *ESP8684 Technical Reference Manual* > Chapter *System and Memory*.

4.1.2.2 External Memory

ESP8684 allows connection to memories outside the chip's package via the SPI, Dual SPI, Quad SPI, and QPI interfaces.

Feature List

- Support connection to off-package flash of 16 MB at most
  - Support hardware encryption/decryption based on XTS-AES
  - Up to 4 MB of CPU instruction memory space can map into flash as individual blocks of 64 KB.
  - Up to 16 MB of CPU data memory space can map into flash as individual blocks of 64 KB.
- External memory accessed via a 16 KB read-only cache
  - Four-way set associative
  - 32-byte cache block
  - Critical word first and early restart

For details, see *ESP8684 Technical Reference Manual* > Chapter *System and Memory*.

4.1.2.3 eFuse Controller

The eFuse memory is a one-time programmable memory that stores parameters and user data, and the eFuse controller of ESP8684 is used to program and read this eFuse memory.

Feature List

- Configure write protection for some blocks
- Configure read protection for some blocks
- Various hardware encoding schemes against data corruption

For details, see *ESP8684 Technical Reference Manual* > Chapter *eFuse Controller*.

4.1.3 System Components

This subsection describes the essential components that contribute to the overall functionality and control of the system.

4.1.3.1 IO MUX and GPIO Matrix

The IO MUX and GPIO Matrix in the ESP8684 chip provide flexible routing of peripheral input and output signals to the GPIO pins. These peripherals enhance the functionality and performance of the chip by allowing the configuration of I/O, support for multiplexing, and signal synchronization for peripheral inputs.

Feature List

- 14 GPIO pins for general-purpose I/O or connection to internal peripheral signals
- GPIO matrix:
  - Routing 33 peripheral input and 61 output signals to any GPIO pin
  - Signal synchronization for peripheral inputs based on IO MUX operating clock
  - GPIO Filter hardware for input signal filtering
- IO MUX for directly connecting certain digital signals (SPI, JTAG, UART) to pins

For details, see *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.1.3.2 Reset

The ESP8684 chip provides four types of reset that occur at different levels, namely CPU Reset, Core Reset, System Reset, and Chip Reset. Except for Chip Reset, all reset types preserve the data stored in internal memory.

Feature List

- Four types of reset:
  - CPU Reset – Resets the CPU core
  - Core Reset – Resets the whole digital system except RTC, including CPU, peripherals, Wi-Fi, Bluetooth® LE, and digital GPIOs
  - System reset – Resets the whole digital system, including RTC
  - Chip reset – Resets the whole chip
- Reset trigger:
  - Directly by hardware
  - Via software by configuring the corresponding registers of the CPU
- Support for retrieving reset cause

For details, see *ESP8684 Technical Reference Manual* > Chapter *Reset and Clock*.

4.1.3.3 Clock

The ESP8684 chip has clocks sourced from external oscillator, RC circuits, and PLL circuits, which are then processed by dividers or selectors. The clocks can be classified into high speed clocks for devices working at higher frequencies and slow speed clocks for low-power systems and some peripherals.

Feature List

- High speed clocks for HP system
  - 480 MHz internal PLL clock
  - 26 MHz or 40 MHz external crystal clock
- Slow speed clocks for LP system and some peripherals working in low-power mode
  - External slow clock (usually 32 kHz)
  - Internal fast RC oscillator with adjustable frequency (17.5 MHz by default)
  - Internal fast RC oscillator divided clock
  - Internal slow RC oscillator with adjustable frequency (136 kHz by default)

For details, see *ESP8684 Technical Reference Manual* > Chapter *Reset and Clock*.

4.1.3.4 Interrupt Matrix

The Interrupt Matrix in the ESP8684 chip routes interrupt requests generated by various peripherals to CPU interrupts.

Feature List

- 43 peripheral interrupt sources accepted as input
- 31 CPU peripheral interrupts generated to CPU as output
- Current interrupt status query of peripheral interrupt sources
- Configurable priority, type, threshold, and enable signal of CPU interrupts

For details, see *ESP8684 Technical Reference Manual* > Chapter *Interrupt Matrix*.

4.1.3.5 System Timer

The System Timer (SYSTIMER) in the ESP8684 chip is a 52-bit timer that can be used to generate tick interrupts for the operating system or as a general timer to generate periodic or one-time interrupts.

Feature List

- Two 52-bit counters and three 52-bit comparators
- 52-bit alarm values and 26-bit alarm periods
- Two modes to generate alarms: target mode and period mode

- Three comparators generating three independent interrupts based on configured alarm value or alarm period
- Software configuring the reference count value. For example, the system timer is able to load back the sleep time recorded by RTC timer via software after Light-sleep
- Able to stall or continue running when CPU stalls or enters on-chip-debugging mode

For details, see *ESP8684 Technical Reference Manual* > Chapter *System Timer*.

4.1.3.6 Power Management Unit

The ESP8684 has an advanced Power Management Unit (PMU). It can be flexibly configured to power up different power domains of the chip to achieve the best balance between chip performance, power consumption, and wakeup latency.

The integrated Ultra-Low-Power (ULP) coprocessors allow the ESP8684 to operate in Deep-sleep mode with most of the power domains turned off, thus achieving extremely low-power consumption.

Configuring the PMU is a complex procedure. To simplify power management for typical scenarios, there are the following **predefined power modes** that power up different combinations of power domains:

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. Wireless base band, and radio are disabled, but wireless connection can remain active.
- Light-sleep mode: The CPU is paused. Any wake-up events (MAC,RTC timer, or external interrupts) will wake up the chip. Wireless connection can remain active.
- Deep-sleep mode: CPU and most peripherals are powered down. Only the PMU in RTC power management unit is powered on. For more details, please refer to Figure 1.

ESP8684 has four power modes, which are predefined configurations that power up different combinations of power domains. For details, please refer to Table 14.

Table 14: Predefined Power Modes

Power Mode	Power Domain					
	PMU	Digital	RC_FAST_CLK	XTAL_CLK	PLL_CLK	RF Circuits
Active	ON	ON	ON	ON	ON	ON
Modem-sleep	ON	ON	ON	ON	ON	OFF
Light-sleep	ON	ON	OFF	OFF	OFF	OFF
Deep-sleep	ON	OFF	OFF	OFF	OFF	OFF

4.1.3.7 Brownout Detector

ESP8684 can periodically monitor the voltage of the power supply, and in the event of abnormal voltage, it is capable of generating interrupts or initiating resets.

Feature List

- Configurable detection threshold

- Configurable reset level

For details, see *ESP8684 Technical Reference Manual* > Chapter *Brownout Detector*.

4.1.3.8 Timer Group

The Timer Group (TIMG) in the ESP8684 chip can be used to precisely time an interval, trigger an interrupt after a particular interval (periodically and aperiodically), or act as a hardware clock. ESP8684 has two timer groups, each consisting of one general-purpose timer and one Main System Watchdog Timer.

Feature List

- 16-bit prescaler
- 54-bit auto-reload-capable up-down counter
- Able to read real-time value of the time-base counter
- Halt, resume, and disable the time-base counter
- Programmable alarm generation
- Timer value reload (auto-reload at an alarm or a software-controlled instant reload)
- RTC slow clock frequency calculation
- Real-time alarm events

For details, see *ESP8684 Technical Reference Manual* > Chapter *Timer Group (TIMG)*.

4.1.3.9 Watchdog Timers

The Watchdog Timers (WDT) in ESP8684 are used to detect and recover from malfunctions. The chip contains two digital watchdog timers: one in the timer group (MWDT) and one in the RTC Module (RWDT).

Feature List

- Digital watchdog timers:
  - Four stages, each with a separately programmable timeout value and timeout action
  - Timeout actions: Interrupt, CPU reset, core reset, system reset (RWDT only)
  - Flash boot protection under SPI Boot mode at stage 0
  - Write protection that makes WDT register read only unless unlocked
  - 32-bit timeout counter
- Analog watchdog timer:
  - Timeout period slightly less than one second
  - Timeout actions: Interrupt, system reset

For details, see *ESP8684 Technical Reference Manual* > Chapter *Watchdog Timers*.

4.1.3.10 System Registers

ESP8684 system registers can be used to control the following peripheral blocks and core modules:

Feature List

- System and memory
- Clock
- Software interrupts
- Peripheral clock gating and reset

For details, see *ESP8684 Technical Reference Manual* > Chapter *System Registers (HP_SYSREG)*.

4.1.3.11 Debug Assistant

The Debug Assistant provides a set of functions to help locate bugs and issues during software debugging. It offers various monitoring capabilities and logging features to assist in identifying and resolving software errors efficiently.

Feature List

- Stack pointer (SP) monitoring
- Program counter (PC) logging before the CPU resets occurs
- CPU debugging status logging

For details, see *ESP8684 Technical Reference Manual* > Chapter *Debug Assistant (ASSIST_DEBUG)*.

4.1.4 Cryptography and Security Component

This subsection describes the security features incorporated into the chip, which safeguard data and operations.

4.1.4.1 ECC Accelerator

The ECC Accelerator accelerates calculations based on the Elliptic Curve Cryptography (ECC) algorithm and ECC-derived algorithms like ECDSA, which offers the advantages of smaller public keys compared to RSA cryptography with equivalent security.

Feature List

- Supports two different elliptic curves (P-192 and P-256)
- Seven working modes that supports Base Point Verification, Base Point Multiplication, Jacobian Point Verification, and Jacobian Point Multiplication
- Interrupt upon completion of calculation

For details, see the *ESP8684 Technical Reference Manual* > Chapter *ECC Accelerator (ECC)*.

4.1.4.2 SHA Accelerator

The SHA Accelerator (SHA) is a hardware device that significantly speeds up the SHA algorithm compared to software-only implementations.

Feature List

- Support for multiple SHA algorithms: SHA-1, SHA-224, and SHA-256
- Two working modes: Typical SHA based on CPU and DMA-SHA based on DMA

For more details, see the *ESP8684 Technical Reference Manual* > Chapter *SHA Accelerator (SHA)*.

4.1.4.3 External Memory Encryption and Decryption

The External Memory Encryption and Decryption (XTS_AES) module in the ESP8684 chip provides security for users' application code and data stored in the external memory (flash).

Feature List

- General XTS-AES algorithm, compliant with IEEE Std 1619-2007
- Software-based manual encryption
- High-speed auto decryption without software's participation
- Encryption and decryption functions jointly enabled/disabled by registers configuration, eFuse parameters, and boot mode

For more details, see the *ESP8684 Technical Reference Manual* > Chapter *External Memory Encryption and Decryption (XTS_AES)*.

4.1.4.4 Random Number Generator

The Random Number Generator (RNG) in the ESP8684 is a true random number generator that generates 32-bit random numbers for cryptographic operations from a physical process.

Feature List

- RNG entropy source
  - Thermal noise from high-speed ADC or SAR ADC
  - An asynchronous clock mismatch

For more details about the Random Number Generator, refer to the *ESP8684 Technical Reference Manual* > Chapter *Random Number Generator (RNG)*.

4.2 Peripherals

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

4.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

4.2.1.1 UART Controller

The UART Controller in the ESP8684 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It supports two UART interfaces.

Feature List

- Full-duplex asynchronous communication
- Configurable baud rate, up to 2.5 Mbaud
- Automatic baud rate detection of input signals
- Data frame format:
  - a START bit
  - data bits, ranging from 5 ~ 8
  - a parity bit
  - stop bits, whose length can be 1, 1.5, or 2 bits
- Special character AT_CMD detection
- Supported protocols: RS485, IrDA
- UART as wake-up source
- Software and hardware flow control
- Three clock sources that can be divided:
  - 40 MHz PLL_F40M_CLK
  - internal fast RC oscillator RC_FAST_CLK
  - external crystal clock XTAL_CLK
- 512 x 8-bit RAM shared by TX FIFOs and RX FIFOs of the two UART controllers

For details, see *ESP8684 Technical Reference Manual* > Chapter *UART Controller (UART, LP_UART)*.

Pin Assignment

For UART, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins* and *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.2.1.2 SPI Controller

ESP8684 series features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can be configured to operate in SPI memory mode and SPI2 can be configured to operate in general-purpose SPI mode.

SPI0 and SPI1 are reserved for system use, and only SPI2 is available for users.

Features of SPI0 and SPI1

- Data is transferred in bytes
- Up to four-line STR reads and writes are supported
- The clock frequency is configurable to a maximum of 60 MHz in STR mode

Features of SPI2 General-purpose SPI (GP-SPI)

- It can operate in master and slave modes
- It supports two-line full-duplex communication and single-/two-/four-line half-duplex communication in both master and slave modes
- The host's clock frequency of SPI2 is configurable. The clock frequency is 40 MHz at most
- Data is transferred in bytes
- The clock polarity (CPOL) and phase (CPHA) are also configurable
- The SPI2 interface can connect to GDMA

For details, see *ESP8684 Technical Reference Manual* > Chapter *SPI Controller (SPI)*.

Pin Assignment

For SPI2, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins* and *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.2.1.3 I2C Controller

The I2C Controller supports communication between the master and slave devices using the I2C bus.

Feature List

- one I2C controller operating in master mode
- Standard mode (100 Kbit/s) and fast mode (400 Kbit/s)
- Up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- Support for 7-bit and 10-bit addressing, as well as dual address mode
- 7-bit broadcast address

For details, see *ESP8684 Technical Reference Manual* > Chapter *I2C Controller (I2C)*.

Pin Assignment

For I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins* and *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.2.1.4 LED PWM Controller

The LED PWM Controller (LEDC) is designed to generate PWM signals for LED control.

Feature List

- Six independent PWM generators
- Maximum PWM duty cycle resolution of 14 bits
- Four independent timers with 14-bit counters, configurable fractional clock dividers and counter overflow values
- Adjustable phase of PWM signal output
- PWM duty cycle dithering
- Automatic duty cycle fading
- PWM signal output in low-power mode (Light-sleep mode)

For details, see *ESP8684 Technical Reference Manual* > Chapter *LED PWM Controller*.

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins* and *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

4.2.2.1 SAR ADC

ESP8684 integrates a Successive Approximation Analog-to-Digital Converter (SAR ADC) to convert analog signals into digital representations.

Feature List

- 12-bit sampling resolution
- Analog voltage sampling from up to five pins
- One DIG ADC controller
  - Provides separate control modules for one-time sampling and multi-channel scanning
  - Supports one-time sampling and multi-channel scanning working simultaneously

- User-defined scanning sequence in multi-channel scanning mode
- Provides two filters with configurable filter coefficient
- Supports threshold monitoring

For more details, see *ESP8684 Technical Reference Manual* > Chapter *On-Chip Sensors and Analog Signal Processing*.

Pin Assignment

The pins for the SAR ADC are multiplexed with GPIO0 ~ GPIO4, JTAG.

For more information about the pin assignment, see Section 2.3 *IO Pins* and *ESP8684 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

4.2.2.2 Temperature Sensor

The Temperature Sensor in the ESP8684 chip allows for real-time monitoring of temperature changes inside the chip.

Feature List

- Measurement range: −40 °C ~ 125 °C
- Software triggering, wherein the data can be read continuously once triggered
- Configurable temperature offset based on the environment to improve the accuracy
- Adjustable measurement range

For more details, see *ESP8684 Technical Reference Manual* > Chapter *On-Chip Sensors and Analog Signal Processing*.

4.3 Wireless Communication

This section describes the chip's wireless communication capabilities, spanning radio technology, Wi-Fi and Bluetooth.

4.3.1 Radio

This subsection describes the fundamental radio technology embedded in the chip that facilitates wireless communication and data exchange.

4.3.1.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, the ESP8684 series integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

4.3.1.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

4.3.1.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

4.3.2 Wi-Fi

This subsection describes the chip's Wi-Fi capabilities, which facilitate wireless communication at a high data rate.

4.3.2.1 Wi-Fi Radio and Baseband

The ESP8684 series Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz bandwidth
- 802.11n 0.4 μs guard interval
- Data rate up to 72.2 Mbps
- RX STBC (single spatial stream)
- Adjustable transmitting power
- Antenna diversity
  ESP8684 series supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

4.3.2.2 Wi-Fi MAC

ESP8684 series implements the full 802.11b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP8684 series Wi-Fi MAC applies the following low-level protocol functions automatically:

- Three virtual Wi-Fi interfaces
- Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- Fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- Transmit opportunity (TXOP)
- Wi-Fi multimedia (WMM)
- CCMP, TKIP, WEP, BIP, WPA2-PSK/WPA2-Enterprise, and WPA3-PSK/WPA3-Enterprise
- Automatic beacon monitoring (hardware TSF)

4.3.2.3 Networking Features

Espressif provides libraries for TCP/IP networking and other networking protocols over Wi-Fi. TLS 1.2 (default) and 1.3 are also supported.

4.3.3 Bluetooth LE

This subsection describes the chip's Bluetooth capabilities, which facilitate wireless communication for low-power, short-range applications.

4.3.3.1 Bluetooth LE PHY

Bluetooth Low Energy radio and PHY in ESP8684 series support:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- Coded PHY for longer range (125 Kbps and 500 Kbps)
- HW listen before talk (LBT)

4.3.3.2 Bluetooth LE Link Controller

Bluetooth Low Energy Link Layer Controller in ESP8684 series supports:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- Multiple advertisement sets
- Simultaneous advertising and scanning
- Adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- Connection parameter update
- High duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- Link layer extended scanner filter policies
- Low duty cycle directed advertising
- Link layer encryption
- LE Ping

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 15 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and normal operation of the device at these or any other conditions beyond those indicated in Section 5.2 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 15: Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
Input power pins [1]	Allowed input voltage	−0.3	3.6	V
I_{output} [2]	Cumulative IO output current	—	730	mA
T_{STORE}	Storage temperature	−40	150	°C

[1] For more information on input power pins, see Section 2.5.1 *Power Pins*.

[2] The chip worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in two domains (VDD3P3_RTC, VDD3P3_CPU) output high logic level to ground.

5.2 Recommended Operating Conditions

Table 16: Recommended Operating Conditions

Parameter [1]	Description	Min	Typ	Max	Unit
VDDA3P3, VDDA, VDD3P3_RTC, VDD3P3_CPU[2]	Recommended input voltage	3.0	3.3	3.6	V
I_{VDD} [3]	Cumulative input current	0.5	—	—	A
T_A	Ambient temperature	−40	—	105	°C

[1] See in conjunction with Section 2.5 *Power Supply*.

[2] If writing to eFuses, the voltage on VDD3P3_CPU should not exceed 3.3 V as the circuits responsible for burning eFuses are sensitive to higher voltages.

[3] If you use a single power supply, the recommended output current is 500 mA or more.

5.3 DC Characteristics (3.3 V, 25 °C)

Table 17: DC Characteristics (3.3 V, 25 °C)

Parameter	Description	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V

V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_EN voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage (CHIP_EN voltage is within the specified range)	−0.3	—	0.25 × VDD[1]	V

[1] VDD – voltage from a power pin of a respective power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

5.4 ADC Characteristics

The measurements in this section are taken with an external 100 nF capacitor connected to the ADC, using DC signals as input, and at an ambient temperature of 25 °C with disabled Wi-Fi.

Table 18: ADC Characteristics

Symbol	Parameter	Min	Max	Unit
DNL (Differential nonlinearity)[1]	ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi off	−1	3	LSB
INL (Integral nonlinearity)		−4	8	LSB
Sampling rate	—	—	100	kSPS[2]

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

ESP-IDF provides a couple of calibration methods for ADC. Results after calibration using hardware + software calibration are shown in Table 19. For higher accuracy, users may apply other calibration methods provided in ESP-IDF, or implement their own.

Table 19: ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 950	-5	5	mV
	ATTEN3, effective measurement range of 0 ~ 2800	-10	10	mV

5.5 Current Consumption

5.5.1 RF Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 20: Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @22 dBm	370
		802.11g, 54 Mbps, @20 dBm	320
		802.11n, HT20, MCS7, @19 dBm	300
	RX	802.11b/g/n, HT20	65

Table 21: Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 20.0 dBm	320
		Bluetooth LE @ 9.0 dBm	190
		Bluetooth LE @ 0 dBm	150
		Bluetooth LE @ –15.0 dBm	90
	RX	Bluetooth LE	62

5.5.2 Current Consumption in Other Modes

Table 22: Current Consumption in Low-Power Modes

Work mode	Description	Typ	Unit
Light-sleep	–	140	μA
Deep-sleep	Only RTC timer is powered on	5	μA
Power off	CHIP_EN is set to low level, and the chip is powered off	1	μA

Table 23: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	80	WFI (Wait-for-Interrupt)	9.4	10.3
		CPU run at full speed	12.1	13.0
	120	WFI (Wait-for-Interrupt)	10.7	11.5
		CPU run at full speed	14.7	15.6

[1] Current consumption when all peripheral clocks are **disabled**.

[2] Current consumption when all peripheral clocks are **enabled**. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

5.6 Reliability

Table 24: Reliability Qualifications

Test Item	Test Conditions	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1] ± 2000 V	JS-001
	CDM (Charge Device Mode)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113
TCT (Temperature Cycling Test)	–65 °C/150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103
LTSL (Low Temperature Storage Life)	–40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The front-end circuit is a 0 Ω resistor.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

6.1 Wi-Fi Radio

Table 25: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

6.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 26: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	21.5	—
802.11b, 11 Mbps	—	21.5	—
802.11g, 6 Mbps	—	21.5	—
802.11g, 54 Mbps	—	19.5	—
802.11n, HT20, MCS0	—	21.0	—
802.11n, HT20, MCS7	—	19.0	—

Table 27: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @21.5 dBm	—	-25.2	-10
802.11b, 11 Mbps, @21.5 dBm	—	-25.2	-10
802.11g, 6 Mbps, @21.5 dBm	—	-20.4	-5
802.11g, 54 Mbps, @19.5 dBm	—	-26.8	-25
802.11n, HT20, MCS0, @21 dBm	—	-21.0	-5
802.11n, HT20, MCS7, @19 dBm	—	-29.0	-27

[1] SL stands for standard limit value.

6.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n.

Table 28: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–99.0	—
802.11b, 2 Mbps	—	–96.5	—
802.11b, 5.5 Mbps	—	–94.0	—
802.11b, 11 Mbps	—	–90.0	—
802.11g, 6 Mbps	—	–94.0	—
802.11g, 9 Mbps	—	–92.0	—
802.11g, 12 Mbps	—	–91.0	—
802.11g, 18 Mbps	—	–89.0	—
802.11g, 24 Mbps	—	–86.0	—
802.11g, 36 Mbps	—	–83.0	—
802.11g, 48 Mbps	—	–78.5	—
802.11g, 54 Mbps	—	–77.0	—
802.11n, HT20, MCS0	—	–92.5	—
802.11n, HT20, MCS1	—	–90.5	—
802.11n, HT20, MCS2	—	–87.5	—
802.11n, HT20, MCS3	—	–84.5	—
802.11n, HT20, MCS4	—	–81.5	—
802.11n, HT20, MCS5	—	–77.5	—
802.11n, HT20, MCS6	—	–75.5	—
802.11n, HT20, MCS7	—	–74.0	—

Table 29: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	-1	—

Table 30: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	16	—

6.2 Bluetooth 5 (LE) Radio

Table 31: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	−24.0 ~ 20.0 dBm

Table 32: Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\,1,\,2,\,..k}$	—	1.0	—	kHz
	Max $\|f_0 - f_n\|$	—	2.3	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.4	—	kHz
	$\|f_1 - f_0\|$	—	1.5	—	kHz
Modulation characteristics	$\Delta\, f1_{avg}$	—	250.2	—	kHz
	Min $\Delta\, f2_{max}$ (for at least 99.9% of all $\Delta\, f2_{max}$)	—	234.4	—	kHz
	$\Delta\, f2_{avg}/\Delta\, f1_{avg}$	—	1.0	—	—
In-band spurious emissions	± 2 MHz offset	—	−32	—	dBm
	± 3 MHz offset	—	−38	—	dBm
	> ± 3 MHz offset	—	−41	—	dBm

Table 33: Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\,1,\,2,\,..k}$	—	3.7	—	kHz
	Max $\|f_0 - f_n\|$	—	1.8	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.5	—	kHz
	$\|f_1 - f_0\|$	—	1.1	—	kHz
Modulation characteristics	$\Delta\, f1_{avg}$	—	500.0	—	kHz
	Min $\Delta\, f2_{max}$ (for at least 99.9% of all $\Delta\, f2_{max}$)	—	460.7	—	kHz

Cont'd on next page

Table 33 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	1.0	—	—
In-band spurious emissions	± 4 MHz offset	—	–40	—	dBm
	± 5 MHz offset	—	–43	—	dBm
	> ± 5 MHz offset	—	–44	—	dBm

Table 34: Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	0.6	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.7	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	0.4	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.7	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.0	—	kHz
	Min $\Delta f1_{max}$ (for at least 99.9% of all$\Delta f2_{max}$)	—	241.0	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–32	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–41	—	dBm

Table 35: Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	0.5	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.6	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	0.2	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.8	—	kHz
Modulation characteristics	$\Delta f2_{avg}$	—	251.3	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	234.5	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–32	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–41	—	dBm

6.2.1 Bluetooth LE RF Receiver (RX) Characteristics

Table 36: Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–98.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	8	—	dB
	F = F0 + 1 MHz	—	-1	—	dB
Adjacent channel selectivity C/I					

Cont'd on next page

Table 36 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	F = F0 – 1 MHz	—	-3	—	dB
	F = F0 + 2 MHz	—	–26	—	dB
	F = F0 – 2 MHz	—	–28	—	dB
	F = F0 + 3 MHz	—	–34	—	dB
	F = F0 – 3 MHz	—	–33	—	dB
	F >= F0 + 4 MHz	—	–33	—	dB
	F <= F0 – 4 MHz	—	–31	—	dB
Image frequency	—	—	–33	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–32	—	dB
	F = F_{image} – 1 MHz	—	–34	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–23	—	dBm
	2003 MHz ~ 2399 MHz	—	–30	—	dBm
	2484 MHz ~ 2997 MHz	—	–10	—	dBm
	3000 MHz ~ 12.75 GHz	—	–17	—	dBm
Intermodulation	—	—	–31	—	dBm

Table 37: Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–95.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	–11	—	dB
	F = F0 – 2 MHz	—	–7	—	dB
	F = F0 + 4 MHz	—	–35	—	dB
	F = F0 – 4 MHz	—	–30	—	dB
	F = F0 + 6 MHz	—	–35	—	dB
	F = F0 – 6 MHz	—	–29	—	dB
	F >= F0 + 8 MHz	—	–39	—	dB
	F <= F0 – 8 MHz	—	–33	—	dB
Image frequency	—	—	–35	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–35	—	dB
	F = F_{image} – 2 MHz	—	–11	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–30	—	dBm
	2003 MHz ~ 2399 MHz	—	–34	—	dBm
	2484 MHz ~ 2997 MHz	—	–19	—	dBm
	3000 MHz ~ 12.75 GHz	—	–28	—	dBm
Intermodulation	—	—	–33	—	dBm

Table 38: Bluetooth LE - Receiver Characteristics - 125 Kbps

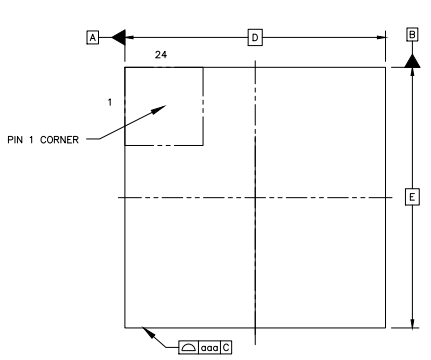
Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–106.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-7	—	dB
	F = F0 – 1 MHz	—	-5	—	dB
	F = F0 + 2 MHz	—	–35	—	dB
	F = F0 – 2 MHz	—	–34	—	dB
	F = F0 + 3 MHz	—	–38	—	dB
	F = F0 – 3 MHz	—	–37	—	dB
	F >= F0 + 4 MHz	—	–41	—	dB
	F <= F0 – 4 MHz	—	–45	—	dB
Image frequency	—	—	–41	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–43	—	dB
	F = F_{image} – 1 MHz	—	–38	—	dB

Table 39: Bluetooth LE - Receiver Characteristics - 500 Kbps

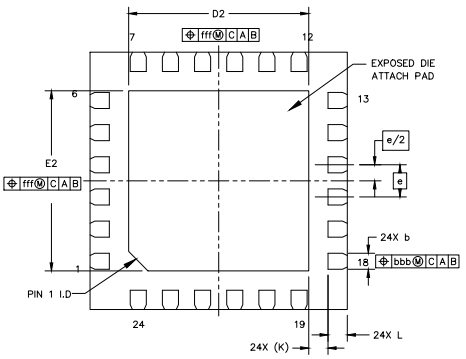
Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–102.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	-6	—	dB
	F = F0 – 1 MHz	—	-5	—	dB
	F = F0 + 2 MHz	—	–29	—	dB
	F = F0 – 2 MHz	—	–32	—	dB
	F = F0 + 3 MHz	—	–31	—	dB
	F = F0 – 3 MHz	—	–36	—	dB
	F >= F0 + 4 MHz	—	–34	—	dB
	F <= F0 – 4 MHz	—	–33	—	dB
Image frequency	—	—	–34	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–37	—	dB
	F = F_{image} – 1 MHz	—	–31	—	dB

7 Packaging

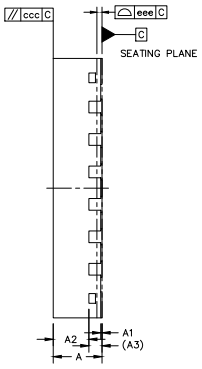
- All dimensions are in millimeters (mm).
- For information about tape, reel, and chip marking, please refer to *ESP8684 Chip Packaging Information*.
- The pins of the chip are numbered in a clockwise order starting from Pin 1 in the top view. For pin numbers and pin names, see also Figure 3 *ESP8684 Pin Layout (Top View)*.
- Please go to Chipsets to view the recommended PCB package source file (asc). The source file can be imported using software such as PADS or AD (Altium Designer);



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

NOTES

1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP · Sn8~20s

Figure 8: QFN24 (4×4 mm) Package

Appendix A – ESP8684 Consolidated Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		Analog Function		IO MUX Function					
				At Reset	After Reset	F0	F1	F0	Type	F1	Type	F2	Type
1	ANT	Analog	-										
2	VDDA3P3	Power	-										
3	VDDA3P3	Power	-										
4	GPIO0	IO	VDD3P3_RTC			GPIO0	ADC1_CH0	GPIO0	I/O/T	**GPIO0**	I/O/T		
5	GPIO1	IO	VDD3P3_RTC			GPIO1	ADC1_CH1	GPIO1	I/O/T	**GPIO1**	I/O/T		
6	GPIO2	IO	VDD3P3_RTC	IE	IE		ADC1_CH2	GPIO2	I/O/T	**GPIO2**	I/O/T	FSPIQ	I1/O/T
7	CHIP_EN	IO	VDD3P3_RTC										
8	GPIO3	IO	VDD3P3_RTC	IE	IE		ADC1_CH3	GPIO3	I/O/T	**GPIO3**	I/O/T		
9	MTMS	IO	VDD3P3_RTC		IE		ADC1_CH4	**MTMS**	I1	GPIO4	I/O/T	FSPIHD	I1/O/T
10	MTDI	IO	VDD3P3_RTC		IE			**MTDI**	I1	GPIO5	I/O/T	FSPIWP	I1/O/T
11	VDD3P3_RTC	Power	-										
12	MTCK	IO	VDD3P3_CPU		IE			**MTCK**	I1	GPIO6	I/O/T	FSPICLK	I1/O/T
13	MTDO	IO	VDD3P3_CPU		IE			**MTDO**	O/T	GPIO7	I/O/T	FSPID	I1/O/T
14	GPIO8	IO	VDD3P3_CPU	IE	IE			GPIO8	I/O/T	**GPIO8**	I/O/T		
15	GPIO9	IO	VDD3P3_CPU	IE	IE, WPU			GPIO9	I/O/T	**GPIO9**	I/O/T		
16	GPIO10	IO	VDD3P3_CPU					GPIO10	I/O/T	**GPIO10**	I/O/T	FSPICS0	I1/O/T
17	VDD3P3_CPU	Power	-										
18	GPIO18	IO	VDD3P3_CPU					GPIO18	I/O/T	**GPIO18**	I/O/T		
19	U0RXD	IO	VDD3P3_CPU		IE, WPU			**U0RXD**	I1	GPIO19	I/O/T		
20	U0TXD	IO	VDD3P3_CPU		OE, WPU			**U0TXD**	O	GPIO20	I/O/T		
21	VDDA	IO	-										
22	XTAL_N	Analog	-										
23	XTAL_P	Analog	-										
24	VDDA	IO	-										
25	GND	Power	-										

* For details, see Section 2 *Pins*. Regarding highlighted cells, see Section 2.3.3 *Restrictions for GPIOs and RTC_GPIOs*.

Datasheet Versioning

Datasheet Version	Status	Watermark	Definition
v0.1 ~ v0.5 (excluding v0.5)	Draft	Confidential	This datasheet is under development for products in the design stage. Specifications may change without prior notice.
v0.5 ~ v1.0 (excluding v1.0)	Preliminary release	Preliminary	This datasheet is actively updated for products in the verification stage. Specifications may change before mass production, and the changes will be documentation in the datasheet's Revision History.
v1.0 and higher	Official release	—	This datasheet is publicly released for products in mass production. Specifications are finalized, and major changes will be communicated via Product Change Notifications (PCN).
Any version	—	Not Recommended for New Design (NRND)[1]	This datasheet is updated less frequently for products not recommended for new designs.
Any version	—	End of Life (EOL)[2]	This datasheet is no longer mtained for products that have reached end of life.

[1] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet are not recommended for new designs.

[2] Watermark will be added to the datasheet title page only when all the product variants covered by this datasheet have reached end of life.

Glossary

strapping pin

A type of GPIO pin used to configure certain operational settings during the chip's power-up, and can be reconfigured as normal GPIO after the chip's reset 23

eFuse parameter

A parameter stored in an electrically programmable fuse (eFuse) memory within a chip. The parameter can be set by programming EFUSE_PGM_DATA*n*_REG registers, and read by reading a register field named after the parameter 23

SPI boot mode

A boot mode in which users load and execute the existing code from SPI flash 24

joint download boot mode

A boot mode in which users can download code into flash via the UART or other interfaces (see Table 12 *Chip Boot Mode Control* > Note), and load and execute the downloaded code from the flash or SRAM 24

eFuse

A one-time programmable (OTP) memory which stores system and user parameters, such as MAC address, chip revision number, flash encryption key, etc. Value 0 indicates the default state, and value 1 indicates the eFuse has been programmed 28

Related Documentation and Resources

Related Documentation

- ESP8684 Technical Reference Manual – Detailed information on how to use the ESP8684 memory and peripherals.
- ESP8684 Hardware Design Guidelines – Guidelines on how to integrate the ESP8684 into your hardware product.
- ESP8684 Series SoC Errata – Descriptions of known errors in ESP8684 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP8684 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP8684
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP8684 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP8684 Series SoCs* – Browse through all ESP8684 SoCs.
  https://espressif.com/en/products/socs?id=ESP8684
- *ESP8684 Series Modules* – Browse through all ESP8684-based modules.
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Revision History

Date	Version	Release notes
2026-01-06	v2.3	Updated the "Ordering Code" to "Part Number" in Table 1 Comparison
2025-07-31	v2.2	Added Section *Crystal Frequency Selection*
2025-02-18	v2.1	• Update the CoreMark score • Add 26 MHz external crystal clock in Section *Clock*
2025-01-21	v2.0	• Update Table *Comparison*: – Update Ordering Code from ESP8684H2 to ESP8684H2X – Update Ordering Code from ESP8684H4 to ESP8684H4X
2024-12-03	v1.9	• Improved the wording and structure of following sections: – Updated Section "Pin Definition" and renamed to *Pins* – Updated Section "Strapping Pins" and renamed to *Boot Configurations* – Updated Chapter *Functional Description* – Updated Table "Wi-Fi RF Standards" and renamed to "Wi-Fi RF Characteristics"
2024-07-01	v1.8	Add descriptions about the relationship between ESP8684 and ESP32-C2 in the title page
2024-03-19	v1.7	Added the first and second table notes in Table 1 *Comparison*
2024-02-07	v1.6	• Updated font to Maison Neue and updated the list format • Added information about Bluetooth 5.3 certification
2024-01-05	v1.5	Removed ESP8684H1 from Table 1
2023-10-31	v1.4	Added current consumption for Bluetooth LE in Active mode in Table *21RF Current Consumption in Active Mode*
2023-07-25	v1.3	• Updated table 1 • Renamed "SiP Flash" to "In-package Flash" to keep term consistency • Updated section 4 *Functional Description* • Updated *Internal Memory*
2022-12-13	v1.2	Updated table *30 Wi-Fi RF Receiver (RX) Characteristics*
2022-12-08	v1.1	Delete feature "Supports external power amplifier"

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Date	Version	Release notes
2022-10-24	v1.0	• Updated section *ADC Characteristics*. • Added section *Reliability*. • Updated section *Bluetooth 5 (LE) Radio* • Added link to the recommended PCB package source file.
2022-07-12	v0.7	Updated section *Peripherals*
2022-06-30	v0.6	Updated *Current Consumption in Other Modes*
2022-05-05	v0.5	Updated *Wi-Fi Radio* and *Bluetooth 5 (LE) Radio*
2022-01-28	v0.4	Updated *Electrical Characteristics* and *Packaging*
2021-12-22	v0.2	Updated section Applications
2021-11-30	v0.1	Preliminary release



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